IN THE CLAIMS:

1. (Currently Amended) A method for determining a plurality of filter coefficients for a digital filter~~, more particularly~~ for the~~a~~ Universal Mobile Telecommunication System (UMTS) ~~(Universal Mobile Telecommunication System)~~, in which the filter coefficients are predetermined and modified in a filter design program, ~~characterized in that~~comprising the steps of:

dividing the predetermined filter coefficients (b_v) ~~are divided~~ by a same scaling factor (s), ~~in that the~~to result in a plurality of scaled filter coefficients (β_v);

quantizing the scaled filter coefficients (β_v) ~~are quantized by this, in~~ so that only a certain maximum number (n) of "1" bits are ~~used~~ counted from ~~the~~a most significant bit onwards and in that ~~the~~a respective quantization error ~~of the~~each quantized scaled filter coefficient is determined relative to the predetermined filter coefficient; and ~~by~~

~~repeated~~repeatedly modifying for a predetermined number of times ~~modification of~~ the scaling factor (s) of ~~the~~a respective scaling factor (s_o) ~~i~~beings set in which the quantization error ~~is~~becomes a predetermined minimal error value, and in that the filter coefficients (β_v) having the minimal error are implemented in the filter.

2. (Currently Amended) A method as claimed in claim 1, characterized in that the number (n) ~~is~~comprises one of four, ~~or~~ three, or two.

3. (Original)A method as claimed in claim 1, characterized in that if again a "1" bit follows the last "1" bit, a rounding is effected from the last bit onwards.

4. (Currently Amended) A digital filter~~, more particularly~~ for a Universal Mobile Telecommunication System (UMTS), in which the digital filter coefficients are processed with the signal, ~~characterized in that~~ comprising

means for dividing ~~the~~a plurality of binary filter coefficients (b_v) ~~are~~ scaled by a scaling factor (s_0) to result in a plurality of scaled filter coefficients (β_v); ;

means for quantizing ~~and in that~~ the filter coefficients (β_v) ~~are quantized~~ so that they do not exceed a ~~certain~~predetermined number (n) of "1" bits from ~~the~~a most significant bit onwards, in that adder stages ADD(3) ~~are provided which process~~ for processing the scaled and quantized filter coefficients (β_q) with the signal.

5. (Currently Amended)~~A~~ The digital filter as claimed in claim ~~14~~, ~~characterized in that the~~ comprising a final stage (4) ~~is provided which processes~~for processing an~~the~~ output signal by a factor (s_0) reciprocal to the scaling factor.

6. (Currently Amended)A digital filter as claimed in claim 4, characterized in that each adder stage (3) comprises n-1 adders (9, 10, 11) and a means for ~~n-squaring multipliers~~ multiplying an input by 2^i by shifting the input by i (5, 6, 7, 8).

7. (Currently Amended) A digital filter as claimed in claim 4, characterized in that in the adder stages (3) and ~~the~~a number n of ~~the squaring multipliers~~a means for multiplying an input by 2^i by shifting the input by i (5, 6, 7, 8) is different and the number of adders (9, 10, 11) is accordingly different.

8. (Currently Amended) A digital filter as claimed in claim 7, characterized in that individual adder stages (3) have only a ~~single squaring multiplier~~ single multiplying means (5).

9. (Currently Amended) A digital filter as claimed in claim ~~14~~, characterized in that the ~~squaring multiplier~~ means for multiplying (5, 6, 7, 8) an input by 2^i by shifting the input by i is formed by connections of its inputs and outputs.

10. (Currently Amended) A digital filter as claimed in claim ~~14~~, characterized in that the adder stage (3) comprises a programmable selector (12) which in accordance with its programming connects the ~~squaring multiplier~~ means for multiplying an input by 2^i by shifting the input by i (5, 6, 7, 8) with the adders (9, 11).

11. (New) The method according to claim 1, further comprising multiplying (5, 6, 7, 8) an input by 2^i by shifting the input by i with a plurality of adders (9, 11).

12. (New) The method according to claim 1, further comprising:

multiplying an input by 2^i by shifting the input by i (5, 6, 7, 8), which is formed by connections of its inputs and outputs.

13. (New) The method according to claim 11, wherein an adders stage (3) comprises a programmable selector (12) which in accordance with its programming connects the shifted input with the adders (9, 11).